Pattern-Based Approach to Current Density Verification

Vazgen Melikyan, Eduard Babayan, Ashot Harutyunyan

Abstract - Methodology of static verification of current density based on layout patterns common in IC designs proposed. The methodology is based on pre-calculation of current density distribution for common layout patterns to use the obtained data to calculate current densities of large circuits partitioning them by selected patterns. The presented experimental results show the effectiveness of the approach.

Keywords – Current density, electromigration, verification, patterns.

I. INTRODUCTION

With increasing technology scaling, physical effects consideration and their impact priorities have changed. In particular, impact of electromigration (EM) increases [1-4]. EM is the mass transport in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms [1]. Electromigration damages interconnects as amounts of matter leaving and entering a given volume are unequal, the associated accumulation or loss of material results in damage [1]. When atomic flux into a region is greater than the flux leaving it, the matter accumulates in the form of a hillock. If the flux leaving the region is greater than the flux entering, the depletion of matter ultimately leads to a void (Fig. 1) [2].

Obviously, EM results in failure of IC which can be result not only of break or short-circuit, but also a significant increase in the interconnect resistance.

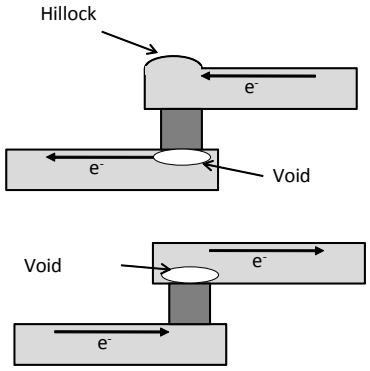

Fig. 1. Hillocks and voids

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EM is defined as [3]:

$$J = -\frac{N_A}{kT} D_0 e^{-\frac{Q}{kT}} eZ^* \rho j \qquad (1)$$

where N_A – density of atoms in the crystal lattice; D_0 – diffusion coefficient; Q – activation energy; eZ^* - resulting charge; ρ - resistivity; k – Boltzmann constant; T – absolute temperature; j – current density.

During IC design it is required to check design against EM possibilities. As it is seen from Eq. (1), EM possibility check can be done by checking current density against maximum allowable current densities. Currently there are different current density verification EDA tools by different vendors. These tools have common disadvantages: they work only on chip level, require additional extraction and simulation steps and large amount of background information, lack error correction, etc. [4,5]

This paper presents methodology of creation of current density verification tool based on common layout patterns which enables high verification performance without need of additional design steps.

II. METHODOLOGY

It is proposed to select common layout patterns (LP), taking into account the frequency of their use in real ICs and relative areas covered by them statistically (Table 1). According to these criteria, the following LPs, shown in Fig. 2 and Table 1 were chosen for modelling.

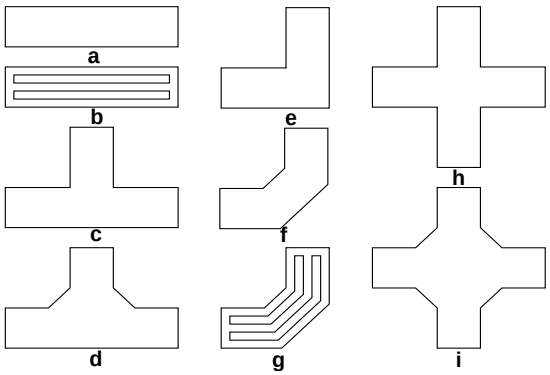

Fig. 2. Common layout patterns selected for modelling

Simulation of these patterns enables automatic estimation of maximum current density in these patterns depending on their geometrical parameters.

TABLE I
STATISTIC DATA FOR PATTERNS SELECTION

LP	IC A		IC B		IC C		IC D	
	Area, %	Count	Area, %	Count	Area, %	Count	Area, %	Count
a.	39	16643910	36	20582714	40	7374407	31	6583941
b.	10	9283	14	16700	0	0	0	0
c.	4	56859	2	13269	9	170152	5	8195
d.	0	0	4	2582	0	0	0	0
e.	16	341139	4	840437	11	166584	15	225007
f.	0	0	12	38474	2	39033	0	5
g.	1	28	1	56	0	0	0	64
h.	3	65401	3	26780	6	95161	2	16339
i.	0	0	5	1341	0	0	0	0
Total	73		81		68		53	

For LP selection current density values in the direction of the normal were taken as boundary conditions. The dependence of the maximum current density on the boundary conditions and geometric parameters of the model was calculated.

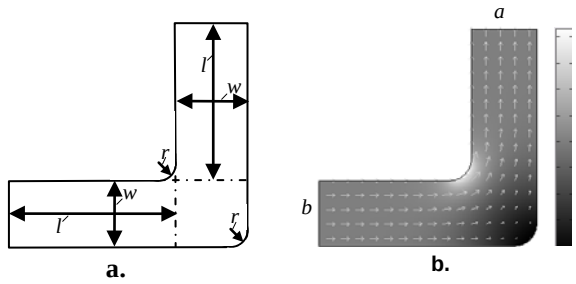

Fig. 3. For modelled LP: a – parameters;
b – current density distribution

The essence of the method is demonstrated below for the example LP in Fig. 3 is shown. In this case currents distribution is uniform in the direction of normal, equal to j_n and $-j_n$ for edges *a* and *b* respectively, and 0 for the rest. Current density distribution map shows that in the inner corner of the LP current is thickened, and on the outside, on the contrary, is diluted. Simulation was performed to identify patterns of current distribution for non-uniform boundary conditions.

For edge *a* of LP in Fig. 4.a, a boundary condition of uniform current distribution $j_n=1$ was set, and current distribution for edge b is shown on Fig.5b and it is mostly concentrated in upper corner. Current density reduces near upper corner and increases near bottom at a distance from edge b. In the middle of the straight segment the densities of these currents are most close to each other (Fig. 5c).

It was found out that with the increase of length of LP branches, the largest and smallest values in Fig.4c tend to 1. Consequently, it can be assumed that when length of

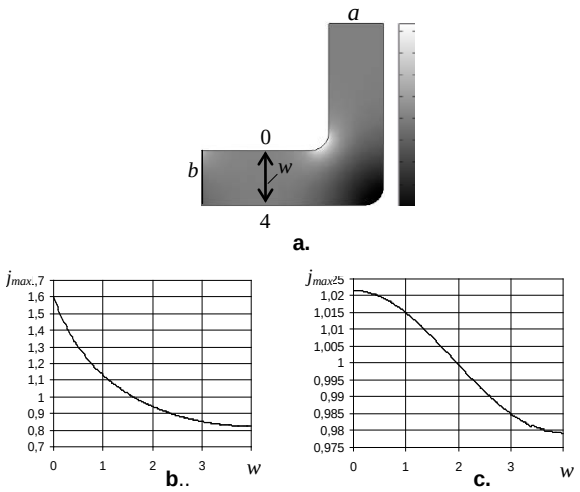

Fig. 4. Uneven distribution of boundary currents

branches *l* decreases in the considered model, the impact boundary conditions distribution on the largest value of current density (LVCD) decreases. This enables to neglect boundary conditions distribution and its impact on current density distribution. The calculation of the boundary currents distribution leads to solution of differential equations. It is required to find a minimum length of branches l_{min} such that for the lengths of the branches above it, the relative difference between the maximum values of current density model does not exceed the specified error ε at all possible *r* and *w*.

The length l_{min} should be found for boundary conditions, which can be assumed the worst from a practical point of view, i.e. for other boundary conditions for the same values of ε smaller values of l_{min} are obtained. As a result of investigations for the considered LP structure shown in Fig. 5 was chosen, which provides the worst boundary conditions.

With the help of the chosen structure, the dependence of l_{min} on the radius *r* and width *w* was found (Fig. 5).

An experiment has been made to find the significance of changes of maximum values of current density, depending on the lengths l_1 and l_2 larger than *l*.

Given that with decrease of length *l* impact of boundary conditions on LVCD increases, the value of *l* was chosen as small as possible $l = 3 \cdot r$ for experiment (this is the smallest, because at $l = 2 \cdot r$ the interior edges are equal to zero (Fig. 5))

The value of *w* was selected equal to *l*. This value of *w* can be viewed as worst practically, because with increase of *w* the impact of boundary conditions on LVCD increases and its error ε is practically unacceptably large. Obviously, the experimental results do not depend on the value of *r*. Taking $r=1$, $l=3$ and $w=3$ values can be obtained. Due to imposition of branches of values of l_1 and l_2 cannot exceed *l*. Thus, the value of one of them is fixed and only the value of another changes. Based on the dependence of LVCD on l_1 obtained through the experiment, it can be

concluded that for l_1 nearly equal l an LVCD is obtained which for larger l_1 is less than LVCD by no more than 1% (Fig. 6).

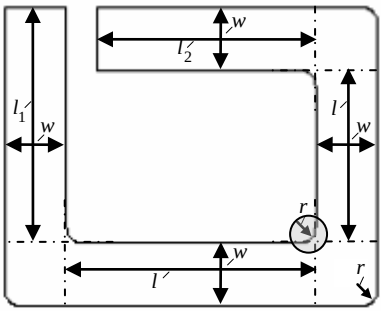

Fig. 5. The selected structure to obtain l_{min}

To find the dependence of LVCD from simultaneous change of l_1 and l_2, first l_1 changed in the range less than l (Fig. 7a), then both changed (Fig.7b). Thus it can be stated that the values found for values larger than l will not change with increase of l_2. Values of l_1 and l_2 can be taken equal to l during calculation of LVCD dependence on considered model parameters.

In the result of experiments it was found out that for worst selected values of $l/w=1.5$, the relative difference of obtained LVCD values is *0.5…0.6%* compared to values obtained for values larger than l (Fig. 8).

For considered LP, with the condition of $l/w \geq 1.5$ experiments were implemented to find the dependence of current densities on parameters r and w.

In the result of previous experiment it was obtained that j_{max} does not depend on w and r and vice versa; thus it can be expressed as:

$$j_{max}=f(r)\cdot\varphi(w)\cdot j, \tag{2}$$

where

$$j=I/w \tag{3}$$

representing current density in uniform area. Thus it is the boundary condition for those edges of the considered LP, which have nonzero current flowing in the direction of normal.

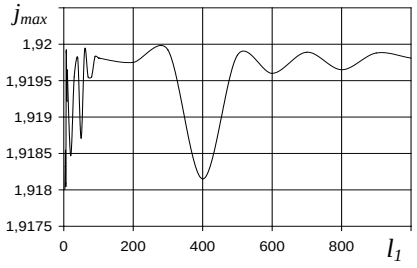

Fig. 6. Dependence of j_{max} on l_1, for $l_1 \geq l$

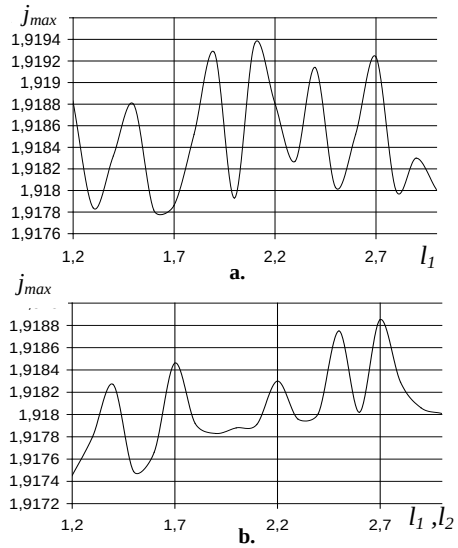

Fig. 7. Dependence of j_{max} a – on l_1, for $l_1 \leq l$, b – on l_1 and l_2 ($l_1 \leq l$, $l_2 \leq l$)

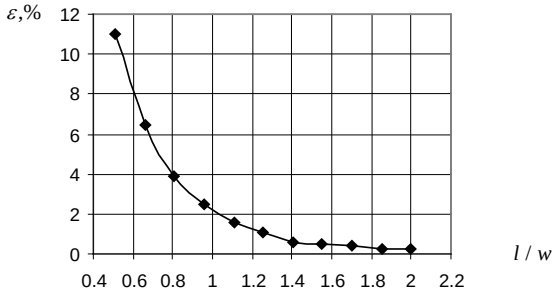

Fig. 8. Dependence of error ε on l/w

To obtain functions f and φ two experiments were implemented resulting in dependencies of jmax on w (Fig. 9a) and r (Fig. 9b) with fixed value of another variable.

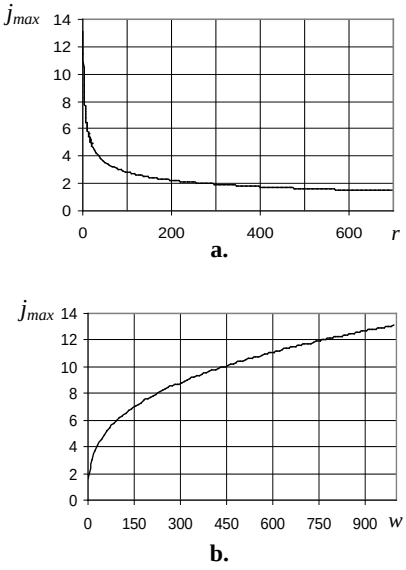

Fig. 9. Dependence of j_{max} on a – w, b – r

In the result of approximation of dependence function, the following was obtained for considered LP:

$$j_{max} = (13{,}2 \cdot r^{-0{,}33} - 0{,}06368) \cdot \cdot (0{,}09743 \cdot w^{0{,}3365} + 0{,}0005986) \cdot j \quad (4)$$

Using expressions Eqs. (2) and (3), for *w* this is obtained:

$$\frac{0{,}09743 \cdot w^{0{,}3365} + 0{,}0005986}{w} = \frac{j_{\max}}{I \cdot (13{,}2 \cdot r^{-0{,}33} - 0{,}06368)} \quad (5)$$

The general flow of developed method of current density verification is presented on Fig. 10.

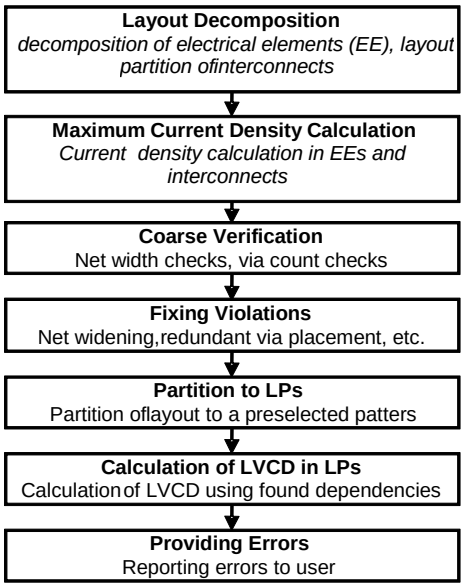

Fig. 10. General current density verification flow

Experimental software implementing the proposed method was developed. Unlike industrial software, it does not need additional extraction and simulation steps. Experimental results are shown in Table 2.

TABLE II.
COMPUTER TIME AND MEMORY REQUIRED TO OBTAIN THE CURRENT DENSITY DISTRIBUTION

Parameters	**Circuit 1**	**Circuit 2**	**Circuit 3**	**Circuit4**
Time, s	0.125	0.391	1.734	7.984
Memory, kB	1.3	8.7	28.9	97.4

For a circuit with 50000 LPs, 104 minutes were required for calculation with conventional software, whereas with proposed method it took only ~10 minutes.

III. CONCLUSION

The developed method of current density verification in ICs and the experimental software package have indisputable advantages over existing similar tools and meet practical requirements of modern IC design.

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